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Appellants' Brief Under 37 C.F.R. 1.192

MS Appeal Brief-Patents
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Dear Sir:

Appellants submit their appeal brief as follows:

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Appellants' Brief Under 37 C.F.R. 1.192

Appellant submit the following brief in support of his appeal.

Real Party In Interest

The assignee of this application, Texas Instruments Incorporated, is the real party in interest in this appeal.

Related Appeals and Interferences

There are no other appeals or interferences that will affect, be affected by or have a bearing on a decision in this appeal.

Status of Claims

Claims 1, 3, 4, 6-12, 14-16, and 18-20 are pending. Applicants appeal the rejection of claims 1, 3, 4, 6-12, 14-16, and 18-20.

Status of Amendments

No amendment has been filed since the last final rejection.

Summary of Invention

The present invention is directed at a method and apparatus for considerably reducing the storage needed in a binary tree search structure.

In a preferred embodiment, an array of values is searched to find the minimum using a binary tree search structure in a storage efficient manner. A plurality of decision units are grouped in a plurality of computation stages. The number of decision units in a computation stage at level i is equal to $N/2^i$, N being the size of the array. Each computation stage reduces by $\frac{1}{2}$ the set of values likely to contain the minimum of the array. Each decision unit in a computation stage takes as its input a pair of data values plus partial addresses of each data value, stores the minimum of the two values and adds to its partial address one most significant bit indicating the local address of the selected data value within the pair of inputs. In this embodiment, each computation stage adds one more bit of address until the entire address is known.

In one embodiment of the present invention, a system for locating a specific value contained in an array of N data values is used. The specific value is the result of a binary operation defined over the array of N data values wherein each data value is W bits wide. The system comprises a plurality of decision units grouped in successive computation stages wherein each decision unit receives a pair of input values, each input value containing a data value and a partial address, and generates values, each input value containing a data value and a partial address, and generates a value representative of a selected data value and the partial address of the selected data value. In

this embodiment, the decision unit of the last computation stage contains the specific value.

In another embodiment, the present invention is related to an apparatus for obtaining information on a specific value within a pair of inputs, wherein each input contains a data value and a partial address of the data value, the apparatus comprising a binary decision representative of a local address of the specific data value and a multiplexer which generates as output the specific data value along with its partial address based on the binary decision.

In yet another embodiment the present invention provides, in an array of N data values, a method of determining an address for a result. The result is the output of a binary operation defined in the array of data values, each data value having W bits. The method comprises the steps of performing, at each computation stage i of $\log_2 N$ computation stages, of $N/2^i$ binary operations on the data values of $N/2$ pairs of input values. In this manner, each of the binary operations generates a binary decision representative of a local address of a selected data value within the pair of input values and multiplexes, at each computation stage, each pair of input values to produce an output determined by the binary decision.

It is an object of the present invention to provide a method for finding a specific value in an array of data values, the method comprising the steps of grouping a plurality of decision units in a plurality of computation stages wherein the number of decision units in computation stage level i is equal to $N/2^i$, N being the size of the array, and processing the data values in each decision unit. A decision unit at a last computation stage determines the specific value.

The present invention can be used in any array having a transitive binary operator defined on it wherein the binary operator maps any pair to the Boolean set of {true, false}.

Issues

There are six issues in this appeal:

1. Whether claims 1, 3, 4, 8, 9, 12, 14-16, and 18-20 are is anticipated by a patent to Dent et al. (5,187,675) pursuant to 35 U.S.C. 102(b).

2. Whether claims 6, 7, 10 and 11 is unpatentable over Dent et al. (5,187,675) under 35 U.S.C. 103(a).

Grouping of Claims

Depending claims 3, 4, 6, 7, and 8 are separately patentable.

Claims 3, 4, 6, 7, and 8 depend from independent Claim 1.

Depending claims 9, 10, and 11 are separately patentable.

Claims 9, 10, and 11 depend from dependent Claim 8 which depends from independent Claim 1.

Depending claims 14 and 15 are separately patentable.

Claims 14 and 15 depend from independent Claim 12.

Depending claims 18-20 are separately patentable.

Claims 18-20 depend from independent Claim 16.

Argument: Issue 1 -- Anticipation of the Claims

The Law

The novelty standard for patentability purposes and the closely related statutory bars are set forth in section 102 of the Patent Act. 35 U.S.C. §102. Novelty refers to whether the invention is considered, as a matter of law, to be in the "public domain" or otherwise as a matter of public policy not entitled to be patented as a result of some type of prior disclosure.

Pursuant to 35 U.S.C. §102(b),

a person shall be entitled to a patent unless
(e) the invention was patented or described
in a printed publication in this or a foreign
country or in public use or on sale in this
country, more than one year prior to the date
of the application for patent in the United
States

In essence, where the publication date of a patent or printed publication which fully and adequately discloses an invention claimed is more than one year prior to the filing date of the instant application, the later application is barred. In addition, if the date of public use or sale of the same invention is more than one year prior to the filing date of the instant application, the later application is barred.

A party asserting that a patent claim is anticipated under 35 USC §102 must demonstrate, among other things, identity of invention. Identity of invention is a question of fact, Coupe v. Royer, 155 U.S. 565, 578-79, 15 S. Ct. 199 (1895). The court in Kalman v. Kimberly-Clark, 218 USPQ 781, 786-787 (Fed. 2d 1983), stipulates:

one who seeks such a finding must show that each element of the claim in issue is found, either expressly described or under principles of inherency, in single prior art reference, or that the claimed invention was previously known or embodied in a single prior art device or practice. Preliminary to this determination, of course, is construction of the claims to determine their meaning in light of the specification and prosecution history, which construction is a matter of law for the court.

Independent Claim 1

Claim 1 recites:

A system for locating a specific value contained in an array of N data values, the specific value being the result of a binary operation defined over the array of N data values wherein each data value is a plurality of bits wide, the system comprising a plurality of decision units grouped in successive computation stages wherein:

(a) each decision unit receives a pair of input values, each input value containing a data value and a partial address; and

(b) each decision unit generates a value representative of a selected data value and the partial address of the selected data value and the decision unit of the last computation stage contains the specific value, wherein each of the plurality of decision units comprises:

(i) a binary operator for generating a binary decision representative of a local address of the selected data value,

(ii) a multiplexer coupled to the binary operator for generating one of the pair of input values as output and with the output being selected by the binary decision, and

(iii) a storage element coupled to the binary operator and the multiplexer for storing the output of the multiplexer and the binary decision which is added to the partial address of the selected data value.

The required structural limitation of the a system for locating a specific value contained in an array of N data values includes a binary operator, a multiplexer and a storage element

as configured in Claim 1 must be shown or taught in the referenced patent, Dent.

As stipulated in the Specification on page 8, lines 11-14, in Figure 1, a decision unit is composed of a binary operator, which is represented here as comparator 101, a multiplexer 103, and storage element 105. To that extent, in the alternative, the required structural limitation of the system of Claim 1 includes a comparator, a multiplexer and a storage element. Thereby, the referenced patent, Dent at least must show or teach this required structural limitation as configured in Claim 1.

Specifically, the "multiplexer coupled to the binary operator for generating one of the pair of input values as output and with the output being selected by the binary decision" must be shown or taught in the referenced patent, Dent. Furthermore, the "a storage element coupled to the binary operator and the multiplexer for storing the output of the multiplexer and the binary decision which is added to the partial address of the selected data value" must be shown or taught in the referenced patent, Dent.

Claim 1: The Dent Patent

Dent et al. teaches a bit-serial MSB-comparator as is shown in Figure 2A. This electronic comparator selects and outputs the larger of the first and second electrical, binary coded input values presented bit-serially, most-significant-bit first, wherein the comparator has first and second input terminals; a logical exclusive-OR gate; a first resettable flip-flop; a second flip-flop; and an input-selector switch, which a device for selecting one of the input values as an output of the comparator.

The second flip-flop generates a traceback signal which controls the device that selects one of the input values as the output of the comparator.

In particular, the bit-serial MSB-first comparator receives a pair of binary-coded values presented bit-serially, MSB first, on inputs A and B to an otherwise conventional exclusive-OR ("XOR") gate that produces a logic HIGH, or "1", output when the values on inputs A and B are unequal. Since the pair of input values are presented and compared bit by bit, MSB first, the input value having the binary "1" will be recognized as the larger on the first occasion that two unlike bits are encountered.

When the output of the XOR gate goes HIGH, indicating that the inputs A, B, are different, it sets the first resettable flip-flop that remains set for the rest of the bits of the pair of input values. The first resettable flip-flop, which may be a conventional set-reset flip-flop, also has a reset input for a suitable control signal for initializing the latch output to logic LOW, or "0", before the first and between sets of input values. The output of the first resettable flip-flop is connected to the clock input of the second flip-flop or D-type flip-flop; thus, when the output of the first resettable flip-flop goes HIGH, the value of one of the inputs (input A, for example) is clocked into the second flip-flop.

In particular, when the input value A is larger than the input value B (e.g., A's MSB is a "1" and B's MSB is a "0"), the Q output of the second flip-flop goes HIGH. Thereby, the Q output acts as a control signal indicated by a dotted line that causes the input-selector switch, such as a field-effect transistor ("FET"), to switch to the "1" position as shown, thereby connecting the input A to the comparator output for the rest of the pair of input values.

On the other hand, if the input A is a "0" when the output of the first resettable flip-flop goes HIGH, the A input is again clocked into the second flip-flop, and the Q output goes LOW, causing the input-selector switch to switch to the "0" position. Thus, the input B is connected to the output for the rest of the pair of input values.

It will be appreciated that the Q output of the second flip-flop indicates which of the two inputs was selected (i.e., which value was "1"), and thus the Q output is provided as the comparator's traceback signal output C.

The comparator may also include an associated traceback-selector switch that couples to receive the traceback signals generated at output C of each unit, as shown in Figure 2A, wherein the traceback-selector switch couples to receive both a first and second traceback signal: A TRACEBACK or B TRACEBACK signal from comparators in preceding tree stages.

In a second embodiment, the electronic comparator has first and second input terminals; a logical exclusive-OR gate; a first flip-flop synchronized with a train of bitclock pulses; a second resettable flip-flop; a third flip-flop; and a device for selecting one of the input values as an output of the comparator. This electronic comparator includes devices for generating traceback signals which indicate which input values were selected and a signal indicating that the maximum value has been identified are also disclosed.

The prior art binary tree structure that is disclosed in Dent et al. teaches is symmetric, or regular when $M=2^N$ for determining the greatest or the least. As shown in Figure 1, pairs of the M input values V_0-V_7 are compared in a first stage of a tree 10 having $M/2=4$ comparators 11-1 to 11-4; the larger value of each pair is selected and passed to a second stage

having $M/4=2$ comparators 12-1, 12-2. The larger values of the two pairs are passed to the final, third stage having $M/8=1$ comparator 13, which passes the largest values V_{MAX} to its output. It will be appreciated that the number of stages needed for searching the M input values is just N .

Dent et al. discloses a known binary tree structure that is symmetric, or regular when $M=2^N$ for determining the greatest or the least. Dent et al. does not teach nor suggest the system that includes the binary operator, the multiplexer nor the storage element as is required by the Claim 1. Clearly, the Dent patent does not teach the configuration as required by Claim 1.

Claim 1 teaches a system the includes a binary operator or comparator, a multiplexer and a storage element configured with the structural limitations as disclosed.

Dent et al. teaches an arrangement for solely a comparator.

Dent et al. does not provide an apparatus with the required features of a system for locating a specific value contained in an array of N data values required by Claim 1. Dent et al. does not teach nor suggest a "multiplexer coupled to the binary operator for generating one of the pair of input values as output and with the output being selected by the binary decision" as required by Claim 1. Furthermore, Dent et al. does not teach nor suggest "a storage element coupled to the binary operator and the multiplexer for storing the output of the multiplexer and the binary decision which is added to the partial address of the selected data value" as required by Claim 1.

Dent et al. does not disclose a storage element.

Dent et al. does not disclose a multiplexer connected to the comparator disclosed. The input-selector switch 108 disclosed in comparator 100 of Figure 2A is not a separate multiplexer unit as required by claim 1.

Dent et al. teaches an arrangement for solely a comparator.

Moreover, since Dent et al. does not show nor suggest the claimed features of Claim 1, Claim 1 is unanticipated and unobvious over Dent et al.

It would not have been obvious at the time the invention was made to a person having ordinary skill in the art to employ in Dent et al. the configuration as is recited in Claim 1 particularly since Dent et al. does not anticipate Claim 1 in that it does not teach each and every limitation as is required by Claim 1. Moreover, since Dent et al. does not show nor suggest the claimed features of amended Claim 1, Claim 1 is unanticipated and unobvious over Dent et al. as recited by Examiner.

Claims 3, 4, 8, 9 depends from Claim 1 and are not anticipated and unobvious over Dent et al. as recited by Examiner pursuant to 35 U.S.C. §102(b) for reasons given above with respect to claim 12.

Depending Claim 3

Dependent Claim 3 is allowable as depending on allowable independent amended Claim 1 and including further limitations that distinguish over the art. Specifically, Claim 3 provides that the binary operator selects the minimum value of the pair of data values contained in the pair of input values.

The Dent patent does not disclose nor suggest a system for locating a specific value contained in an array of N data values as required by Claim 3.

Depending Claim 4

Dependent Claim 4 is allowable as depending on allowable independent amended Claim 1 and including further limitations that distinguish over the art. Specifically, Claim 4 provides that the binary operator selects the maximum value of the pair of data values contained in the pair of input values.

The Dent patent does not disclose nor suggest a system for locating a specific value contained in an array of N data values as required by Claim 4.

Depending Claim 8

Dependent Claim 8 is allowable as depending on allowable independent amended Claim 1 and including further limitations that distinguish over the art. Specifically, claim 8 at least provides claim differentiation.

The Dent patent does not disclose nor suggest a system for locating a specific value contained in an array of N data values as required by Claim 8.

Depending Claim 9

Dependent Claim 9 is allowable as depending on allowable dependent Claim 8 which depends from independent claim 1 and including further limitations that distinguish over the art. Specifically, claim 9 at least provides claim differentiation.

The Dent patent does not disclose nor suggest a system for locating a specific value contained in an array of N data values as required by Claim 9.

Independent Claim 12

Claim 12 recites:

An apparatus for obtaining information on a specific value within a pair of inputs, wherein each input contains a data value and a partial address of the data value, the apparatus comprising:

(a) a binary operator which compares the data values and which generates as output a binary decision representative of a local address of the specific data value;

(b) a multiplexer coupled to the binary operator and coupled to receive each data values along with its partial address which generates as output the specific data value along with its partial address based on the binary decision; and

(c) a storage element coupled to the binary operator and the multiplexer which stores the output of the multiplexer and the binary decision.

The required structural limitation of the system for locating a specific value contained in an array of N data values includes a binary operator, a multiplexer and a storage element as configured in Claim 12 must be shown or taught in the referenced patent, Dent.

Specifically, the "multiplexer coupled to the binary operator for generating one of the pair of input values as output and with the output being selected by the binary decision" must be shown or taught in the referenced patent, Dent. Furthermore, the "a storage element coupled to the binary operator and the multiplexer for storing the output of the multiplexer and the binary decision which is added to the partial address of the selected data value" must be shown or taught in the referenced patent, Dent.

Claim 12: The Dent Patent

Following the argument of Claim 1, Dent et al. teaches a bit-serial MSB-comparator that selects and outputs the larger of the first and second electrical, binary coded input values presented bit-serially, most-significant-bit first, wherein the comparator has first and second input terminals; a logical exclusive-OR gate; a first resettable flip-flop; a second flip-flop; and an input-selector switch, which a device for selecting one of the input values as an output of the comparator. The second flip-flop generates a traceback signal which controls the device that selects one of the input values as the output of the comparator.

Furthermore, Dent et al. discloses a prior art binary tree structure that is symmetric, or regular when $M=2^N$ for determining the greatest or the least, wherein the bit-serial MSB-comparator is substituted for each comparator.

Claim 12 teaches a system the includes a binary operator or comparator, a multiplexer and a storage element configured with the structural limitations as disclosed.

Dent et al. teaches an arrangement for solely a comparator.

Dent et al. does not disclose a storage element.

Dent et al. does not disclose a multiplexer connected to the comparator disclosed. The input-selector switch 108 disclosed in comparator 100 of Figure 2A is not a separate multiplexer unit as required by claim 1.

Dent et al. teaches an arrangement for solely a comparator.

Thereby, Dent et al. teaches a binary tree structure that is symmetric, or regular when $M=2^N$ for determining the greatest or the least. Dent et al. does not teach nor suggest the binary operator, the multiplexer nor the storage element as is required by the Claim 12. Clearly, the Dent patent does not teach the configuration as required by Claim 12.

Dent et al. does not provide an apparatus for obtaining information on a specific value within a pair of inputs required by Claim 12. Dent et al. does not teach nor suggest a "multiplexer coupled to the binary operator and coupled to receive each data values along with its partial address which generates as output the specific data value along with its partial address based on the binary decision" as required by Claim 12. Furthermore, Dent et al. does not teach nor suggest "a storage element coupled to the binary operator and the multiplexer which stores the output of the multiplexer and the binary decision" as required by Claim 12.

Moreover, since Dent et al. does not show nor suggest the apparatus of Claim 12, Claim 12 is unanticipated over Dent et al.

It would not have been obvious at the time the invention was made to a person having ordinary skill in the art to employ in Dent et al. the configuration as is recited in Claim 12 particularly since Dent et al. does not anticipate Claim 12 in that it does not teach each and every limitation as is required by Claim 12. Moreover, since Dent et al. does not show nor suggest the claimed features of amended Claim 12, Claim 12 is unanticipated and unobvious over Dent et al. as recited by Examiner.

Claims 14 and 15 depend from Claim 12 and are not anticipated and unobvious over Dent et al. as recited by Examiner pursuant to 35 U.S.C. §102(b) for reasons given above with respect to claim 12.

Depending Claim 14

Dependent Claim 14 is allowable as depending on allowable independent amended Claim 12 and including further limitations that distinguish over the art. Specifically, claim 14 at least provides claim differentiation.

The Dent patent does not disclose nor suggest a system for locating a specific value contained in an array of N data values as required by Claim 14.

Depending Claim 15

Dependent Claim 15 is allowable as depending on allowable independent amended Claim 12 and including further limitations that distinguish over the art. Specifically, Claim 15 at least provides claim differentiation.

The Dent patent does not disclose nor suggest a system for locating a specific value contained in an array of N data values as required by Claim 15.

Independent Claim 16

Claim 16 recites:

In an array of N data values, a method of determining an address for a result, the result being the output of a binary operation defined in the array of data values each data value having W bits, the method comprising the steps of:

(a) performing, at each computation stage i of $\log_2 N$, computation stages, $N/2^i$ binary operations on the data values of $N/2^i$ pairs of input values using a binary operator, wherein each input value includes a data value and

a partial address, wherein each of the binary operations generates a binary decision representative of a selected data value and the partial address of the selected data value;

(b) multiplexing at each computation stage each pair of input values using a multiplexer and producing an output determined by the binary decision; and

(c) storing at each computation stage the binary decision and the selected data value in a storage element.

The required structural limitation of the A system for locating a specific value contained in an array of N data values includes a binary operator, a multiplexer and a storage element as configured in Claim 16 must be shown or taught in the referenced patent, Dent.

Specifically, the "multiplexer coupled to the binary operator for generating one of the pair of input values as output and with the output being selected by the binary decision" must be shown or taught in the referenced patent, Dent. Furthermore, the "a storage element coupled to the binary operator and the multiplexer for storing the output of the multiplexer and the binary decision which is added to the partial address of the selected data value" must be shown or taught in the referenced patent, Dent.

Claim 16: The Dent Patent

Following the previously disclosed issues, Dent et al. teaches a bit-serial MSB-comparator that selects and outputs the larger of the first and second electrical, binary coded input values presented bit-serially, most-significant-bit first, wherein the comparator has first and second input terminals; a logical exclusive-OR gate; a first resettable flip-flop; a second flip-flop; and an input-selector switch, which a device for selecting one of the input values as an output of the comparator.

The second flip-flop generates a traceback signal which controls the device that selects one of the input values as the output of the comparator.

Furthermore, Dent et al. discloses a prior art binary tree structure that is symmetric, or regular when $M=2^N$ for determining the greatest or the least, wherein the bit-serial MSB-comparator is substituted for each comparator.

Claim 16 teaches a method of determining an address for a result, wherein the system that performs this method includes a binary operator or comparator, a multiplexer and a storage element configured with the structural limitations as disclosed.

Dent et al. teaches an arrangement for solely a comparator.

Dent et al. does not disclose a storage element.

The input-selector switch 108 disclosed in comparator 100 of Figure 2A is not a separate multiplexer unit as required by claim 1. Thereby, Dent et al. does not disclose a multiplexer connected to the comparator disclosed.

In particular, Claim 16 requires that "the binary operations generates a binary decision representative of a selected data value", thereby, the binary operator must provide a binary decision.

Dent et al. teaches a comparator that provides a binary decision.

However, Dent et al. fails to teach a multiplexer coupled to the output of the comparator.

Moreover, Dent et al. fails to teach a storage element connected to the multiplexer.

Thereby, Dent et al. teaches a binary tree structure that is symmetric, or regular when $M=2^N$ for determining the greatest or the least. Dent et al. does not teach nor suggest the binary operator, the multiplexer nor the storage element as is required by the Claim 16. Clearly, the Dent patent does not teach the configuration as required by Claim 16.

Claim 16 requires the step of "performing, at each computation stage i of $\log_2 N$, computation stages, $N/2^i$ binary operations on the data values of $N/2^i$ pairs of input values using a binary operator, wherein each input value includes a data value and a partial address, wherein each of the binary operations generates a binary decision representative of a selected data value and the partial address of the selected data value."

Dent et al. does not teach an input value that includes a data value and a partial address.

Furthermore, amended Claim 16 requires the step of "multiplexing at each computation stage each pair of input values using a multiplexer and producing an output determined by the binary decision."

Dent et al. does not teach nor suggest a multiplexer nor the multiplexing step as required by amended Claim 16.

Moreover, amended Claim 16 requires the step of storing at each computation stage the binary decision and the selected input in a storage element.

Dent et al. does not teach nor suggest the storing step nor the storage element.

Claims 18 through 20 depend from Claim 16 and are not anticipated and unobvious over Dent et al. as recited by Examiner pursuant to 35 U.S.C. §102(b) for reasons given above with respect to claim 16.

Depending Claim 18

Dependent Claim 18 is allowable as depending on allowable independent amended Claim 16 and including further limitations that distinguish over the art. Specifically, Claim 18 provides that the computation stage at level $\log_2 N$ contains the value of the result of the binary operation and its address within the array of values. Claim 20 at least provides claim differentiation.

The Dent patent does not disclose nor suggest a system for locating a specific value contained in an array of N data values as required by Claim 18.

Depending Claim 19

Dependent Claim 19 is allowable as depending on allowable independent amended Claim 16 and including further limitations that distinguish over the art. Specifically, Claim 19 at least provides claim differentiation.

The Dent patent does not disclose nor suggest a system for locating a specific value contained in an array of N data values as required by Claim 19.

Depending Claim 20

Dependent Claim 20 is allowable as depending on allowable independent amended Claim 16 and including further limitations that distinguish over the art. Specifically, Claim 20 at least provides claim differentiation.

The Dent patent does not disclose nor suggest a system for locating a specific value contained in an array of N data values as required by Claim 20.

Argument: Issue 2 -- Patentability of the Claims

The Law

The novelty standard for patentability purposes and the closely related statutory bars are set forth in section 102 of the Patent Act. 35 U.S.C. §102. Novelty refers to whether the invention is considered, as a matter of law, to be in the "public domain" or otherwise as a matter of public policy not entitled to be patented as a result of some type of prior disclosure.

Pursuant to 35 U.S.C. §103(a),

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall

not be negated by the manner in which the invention was made.

The obviousness standard, as relayed in MPEP § 2143, requires that the Examiner establish a prima facie case of obviousness to assert a §103 obviousness rejection of a claim. The prima facie case consists of three basic criteria. First, there must be some suggestion or motivation, either in the reference themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference or references when combined must teach or suggest each and every claim limitation.

Depending Claim 6

Claim 6 recites:

The system of claim 1, wherein the partial address of an input value at computation stage i is the $(i-1)$ most significant bit of the storage element of computation stage $(i-1)$.

The invention of the Claim 6 requires that "the partial address of an input value at computation stage i is the $(i-1)$ most significant bit of the storage element of computation stage $(i-1)$."

Claim 6: The Dent Patent

Following the argument of Claim 1, Dent et al. teaches a bit-serial MSB-comparator that selects and outputs the larger of the first and second electrical, binary coded input values presented bit-serially, most-significant-bit first, wherein the comparator has first and second input terminals; a logical exclusive-OR gate; a first resettable flip-flop; a second flip-flop; and an input-selector switch, which a device for selecting

one of the input values as an output of the comparator. The second flip-flop generates a traceback signal which controls the device that selects one of the input values as the output of the comparator.

Furthermore, Dent et al. discloses a prior art binary tree structure that is symmetric, or regular when $M=2^N$ for determining the greatest or the least, wherein the bit-serial MSB-comparator is substituted for each comparator.

Claim 6 teaches a system that includes a binary operator or comparator, a multiplexer and a storage element configured with the structural limitations as disclosed.

Dent et al. teaches an arrangement for solely a comparator.

Dent et al. does not disclose a storage element.

Dent et al. does not disclose a multiplexer connected to the comparator disclosed. The input-selector switch 108 disclosed in comparator 100 of Figure 2A is not a separate multiplexer unit as required by claim 6.

Dent et al. teaches an arrangement for solely a comparator.

Thereby, Dent et al. teaches a binary tree structure that is symmetric, or regular when $M=2^N$ for determining the greatest or the least. Dent et al. does not teach nor suggest the binary operator, the multiplexer nor the storage element as is required by the Claim 6. Clearly, the Dent patent does not teach the configuration as required by Claim 6.

Moreover, since Dent et al. does not show nor suggest the apparatus of Claim 6, Claim 6 is unanticipated over Dent et al.

Dent et al. does not provide an apparatus with the required features of a system for locating a specific value contained in an array of N data values required by Claim 1. Dent et al. does not teach nor suggest a "multiplexer coupled to the binary operator for generating one of the pair of input values as output and with the output being selected by the binary decision" as required by Claim 1. Furthermore, Dent et al. does not teach nor suggest "a storage element coupled to the binary operator and the multiplexer for storing the output of the multiplexer and the binary decision which is added to the partial address of the selected data value" as required by Claim 1.

Moreover, since Dent et al. does not show nor suggest the claimed features of Claim 1, Claim 1 is unanticipated and unobvious over Dent et al.

It would not have been obvious at the time the invention was made to a person having ordinary skill in the art to employ in Dent et al. the configuration as is recited in Claim 1 particularly since Dent et al. does not anticipate Claim 1 in that it does not teach each and every limitation as is required by Claim 1. Moreover, since Dent et al. does not show nor suggest the claimed features of amended Claim 1, Claim 1 is unanticipated and unobvious over Dent et al. as recited by Examiner.

Claims 6 depends from Claim 1 and is not anticipated and unobvious over Dent et al. as recited by Examiner pursuant to 35 U.S.C. §103(a) for reasons given above with respect to Claim 1.

Specifically, dependent Claim 6 is allowable as depending on allowable independent amended Claim 1 and including further limitations that distinguish over the art. In particular, Claim 6 provides that the partial address of an input value at computation stage i is the $(i-1)$ most significant bit of the storage element of computation stage $(i-1)$.

The Dent patent does not disclose nor suggest a system for locating a specific value contained in an array of N data values as required by Claim 6.

Since the Dent et al. patent does not show nor suggest the claimed features, Claim 6 is unanticipated.

Depending Claim 7

Claim 7 recites:

The system of claim 1, wherein the partial address of an input value at computation stage i is the $(i-1)$ least significant bit of the storage element of computation stage $(i-1)$.

The invention of the Claim 7 requires that "the partial address of an input value at computation stage i is the $(i-1)$ least significant bit of the storage element of computation stage $(i-1)$."

Claim 7: The Dent Patent

Following the argument given for independent Claim 1, Dent et al. teaches a binary tree structure that is symmetric, or regular when $M=2^N$ for determining the greatest or the least. Dent et al. does not teach nor suggest the binary operator, the multiplexer nor the storage element as is required by the Claim

1. Clearly, the Dent patent does not teach the configuration as required by Claim 1.

Dent et al. does not provide an apparatus with the required features of a system for locating a specific value contained in an array of N data values required by Claim 1. Dent et al. does not teach nor suggest a "multiplexer coupled to the binary operator for generating one of the pair of input values as output and with the output being selected by the binary decision" as required by Claim 1. Furthermore, Dent et al. does not teach nor suggest "a storage element coupled to the binary operator and the multiplexer for storing the output of the multiplexer and the binary decision which is added to the partial address of the selected data value" as required by Claim 1.

Moreover, since Dent et al. does not show nor suggest the claimed features of Claim 1, Claim 1 is unanticipated and unobvious over Dent et al.

It would not have been obvious at the time the invention was made to a person having ordinary skill in the art to employ in Dent et al. the configuration as is recited in Claim 1 particularly since Dent et al. does not anticipate Claim 1 in that it does not teach each and every limitation as is required by Claim 1. Moreover, since Dent et al. does not show nor suggest the claimed features of amended Claim 1, Claim 1 is unanticipated and unobvious over Dent et al. as recited by Examiner.

Claims 7 depends from Claim 1 and is not anticipated and unobvious over Dent et al. as recited by Examiner pursuant to 35 U.S.C. §103(a) for reasons given above with respect to Claim 1.

Specifically, dependent Claim 7 is allowable as depending on allowable independent amended Claim 1 and including further limitations that distinguish over the art. In particular, Claim 7 provides that the partial address of an input value at computation stage i is the $(i-1)$ least significant bit of the storage element of computation stage $(i-1)$.

The Dent patent does not disclose nor suggest a system for locating a specific value contained in an array of N data values as required by Claim 7.

Since the Dent et al. patent does not show nor suggest the claimed features, Claim 7 is unanticipated.

Depending Claim 10

Claim 10 recites:

The system of Claim 8 wherein the last computation stage contains the address of the specific value in the K most significant bits of its associated storage element and the specific value is contained in the W least significant bits of said associated storage element.

The invention of the Claim 10 requires that "the last computation stage contains the address of the specific value in the K most significant bits of its associated storage element and the specific value is contained in the W least significant bits of said associated storage element."

Claim 10: The Dent Patent

Following the argument given for independent Claim 1, Dent et al. teaches a binary tree structure that is symmetric, or regular when $M=2^N$ for determining the greatest or the least. Dent et al. does not teach nor suggest the binary operator, the multiplexer nor the storage element as is required by the Claim

1. Clearly, the Dent patent does not teach the configuration as required by Claim 1.

Dent et al. does not provide an apparatus with the required features of a system for locating a specific value contained in an array of N data values required by Claim 1. Dent et al. does not teach nor suggest a "multiplexer coupled to the binary operator for generating one of the pair of input values as output and with the output being selected by the binary decision" as required by Claim 1. Furthermore, Dent et al. does not teach nor suggest "a storage element coupled to the binary operator and the multiplexer for storing the output of the multiplexer and the binary decision which is added to the partial address of the selected data value" as required by Claim 1.

Moreover, since Dent et al. does not show nor suggest the claimed features of Claim 1, Claim 1 is unanticipated and unobvious over Dent et al.

It would not have been obvious at the time the invention was made to a person having ordinary skill in the art to employ in Dent et al. the configuration as is recited in Claim 1 particularly since Dent et al. does not anticipate Claim 1 in that it does not teach each and every limitation as is required by Claim 1. Moreover, since Dent et al. does not show nor suggest the claimed features of amended Claim 1, Claim 1 is unanticipated and unobvious over Dent et al. as recited by Examiner.

Claims 10 depends from dependent Claim 8 which depends from independent Claim 1 and is not anticipated and unobvious over Dent et al. as recited by Examiner pursuant to 35 U.S.C. §103(a) for reasons given above with respect to Claim 1.

Specifically, dependent Claim 10 is allowable as depending on allowable independent amended Claim 1 and including further limitations that distinguish over the art. In particular, Claim 10 provides that the last computation stage contains the address of the specific value in the K most significant bits of its associated storage element.

The Dent patent does not disclose nor suggest a system for locating a specific value contained in an array of N data values as required by Claim 10.

Since the Dent et al. patent does not show nor suggest the claimed features, Claim 10 is unanticipated.

Depending Claim 11

Claim 11 recites:

The system of claim 1, wherein the partial address of an input value at computation stage i is the (i-1) least significant bit of the storage element of computation stage (i-1).

The invention of the Claim 11 requires that "the partial address of an input value at computation stage i is the (i-1) least significant bit of the storage element of computation stage (i-1)."

Claim 11: The Dent Patent

Following the argument given for independent Claim 1, Dent et al. teaches a binary tree structure that is symmetric, or regular when $M=2^N$ for determining the greatest or the least. Dent et al. does not teach nor suggest the binary operator, the multiplexer nor the storage element as is required by the Claim

1. Clearly, the Dent patent does not teach the configuration as required by Claim 1.

Dent et al. does not provide an apparatus with the required features of a system for locating a specific value contained in an array of N data values required by Claim 1. Dent et al. does not teach nor suggest a "multiplexer coupled to the binary operator for generating one of the pair of input values as output and with the output being selected by the binary decision" as required by Claim 1. Furthermore, Dent et al. does not teach nor suggest "a storage element coupled to the binary operator and the multiplexer for storing the output of the multiplexer and the binary decision which is added to the partial address of the selected data value" as required by Claim 1.

Moreover, since Dent et al. does not show nor suggest the claimed features of Claim 1, Claim 1 is unanticipated and unobvious over Dent et al.

It would not have been obvious at the time the invention was made to a person having ordinary skill in the art to employ in Dent et al. the configuration as is recited in Claim 1 particularly since Dent et al. does not anticipate Claim 1 in that it does not teach each and every limitation as is required by Claim 1. Moreover, since Dent et al. does not show nor suggest the claimed features of amended Claim 1, Claim 1 is unanticipated and unobvious over Dent et al. as recited by Examiner.

Claims 11 depends from dependent Claim 8 which depends from independent Claim 1 and is not anticipated and unobvious over Dent et al. as recited by Examiner pursuant to 35 U.S.C. §103(a) for reasons given above with respect to Claim 1.

Specifically, dependent Claim 11 is allowable as depending on allowable independent amended Claim 1 and including further limitations that distinguish over the art. In particular, Claim 11 provides that the last computation stage contains the address of the specific value in the K least significant bits of its associated storage element.

The Dent patent does not disclose nor suggest a system for locating a specific value contained in an array of N data values as required by Claim 11.

Since the Dent et al. patent does not show nor suggest the claimed features, Claim 11 is unanticipated.

Conclusion

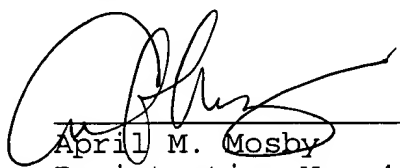
The rejection fails to address the limitations of the claims. Reconsideration and allowance of Claims 1, 3, 4, 6-12, 14-16, and 18-20.

Claims 1, 3, 4, 6-12, 14-16, and 18-20 stand allowable.

Applicants have carefully reviewed the additional references made of record by the Examiner and not relied upon for rejecting the claims, U.S. Patent Nos. 4,821,290, 5,455,825, 4,100,532, 5,710,562, and 5,383,142. Applicants believe that none of these references, taken singly or in any permissible combination, affect the assertion of patentability of claims 1, 3, 4, 6-12, 14-16, and 18-20 in the present application.

The claims 1, 3, 4, 6-12, 14-16, and 18-20 distinguish over the cited references and the application is in allowable form. Applicant respectfully requests reconsideration or further examination and allowance of the application.

Respectfully submitted,



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Appendix

The following claims are on appeal:

1 1. (previously presented) A system for locating a specific value
2 contained in an array of N data values, the specific value being
3 the result of a binary operation defined over the array of N data
4 values wherein each data value is a plurality of bits wide, the
5 system comprising a plurality of decision units grouped in
6 successive computation stages wherein:

7 (a) each decision unit receives a pair of input values, each
8 input value containing a data value and a partial address; and

9 (b) each decision unit generates a value representative of a
10 selected data value and the partial address of the selected data
11 value and the decision unit of the last computation stage
12 contains the specific value, wherein each of the plurality of
13 decision units comprises:

14 (i) a binary operator for generating a binary decision
15 representative of a local address of the selected data value,

16 (ii) a multiplexer coupled to the binary operator for
17 generating one of the pair of input values as output and with the
18 output being selected by the binary decision, and

19 (iii) a storage element coupled to the binary operator
20 and the multiplexer for storing the output of the multiplexer and
21 the binary decision which is added to the partial address of the
22 selected data value.

1 2. (canceled)

1 3. (previously presented) The system of claim 1, wherein the
2 binary operator selects the minimum value of the pair of data
3 values contained in the pair of input values.

1 4. (previously presented) The system of claim 1, wherein the
2 binary operator selects the maximum value of the pair of data
3 values contained in the pair of input values.

1 5. (canceled)

1 6. (previously presented) The system of claim 1, wherein the
2 partial address of an input value at computation stage i is the
3 $(i-1)$ most significant bit of the storage element of computation
4 stage $(i-1)$.

1 7. (previously presented) The system of claim 1, wherein the
2 partial address of an input value at computation stage i is the
3 $(i-1)$ least significant bit of the storage element of computation
4 stage $(i-1)$.

1 8. (original) The system of Claim 1 wherein the number of
2 computation stages K is related to the size N of the array of
3 data values by the formula $K=\log_2 N$.

1 9. (original) The system of Claim 8 wherein the number of
2 decision unites at a computation stage i is equal to $N/2^i$ and
3 wherein $1 \leq i \leq K$.

1 10. (original) The system of Claim 8 wherein the last computation
2 stage contains the address of the specific value in the K most
3 significant bits of its associated storage element and the
4 specific value is contained in the W least significant bits of
5 said associated storage element.

1 11. (original) The system of Claim 8 wherein the last computation
2 stage contains the address of the specific value in the K least
3 significant bits of its associated storage element and the

4 specific value is contained in the W most significant bits of
5 said associated storage element.

1 12. (previously presented) An apparatus for obtaining information
2 on a specific value within a pair of inputs, wherein each input
3 contains a data value and a partial address of the data value,
4 the apparatus comprising:

5 (a) a binary operator which compares the data values and
6 which generates as output a binary decision representative of a
7 local address of the specific data value;

8 (b) a multiplexer coupled to the binary operator and coupled
9 to receive each data values along with its partial address which
10 generates as output the specific data value along with its
11 partial address based on the binary decision; and

12 (c) a storage element coupled to the binary operator and the
13 multiplexer which stores the output of the multiplexer and the
14 binary decision.

1 13. (canceled)

1 14. (original) The apparatus of Claim 12 wherein the binary
2 operator is a minimum operator.

1 15. (original) The apparatus of Claim 12 wherein the binary
2 operator is a maximum operator.

1 16. (previously presented) In an array of N data values, a method
2 of determining an address for a result, the result being the
3 output of a binary operation defined in the array of data values
4 each data value having W bits, the method comprising the steps
5 of:

6 (a) performing, at each computation stage i of $\log_2 N$,
7 computation stages, $N/2^i$ binary operations on the data values of

8 $N/2^i$ pairs of input values using a binary operator, wherein each
9 input value includes a data value and a partial address, wherein
10 each of the binary operations generates a binary decision
11 representative of a selected data value and the partial address
12 of the selected data value;

13 (b) multiplexing at each computation stage each pair of
14 input values using a multiplexer and producing an output
15 determined by the binary decision; and

16 (c) storing at each computation stage the binary decision
17 and the selected data value in a storage element.

1 17. (canceled)

1 18. (original) The method of Claim 16 wherein the computation
2 stage at level $\log_2 N$ contains the value of the result of the
3 binary operation and its address within the array of values.

1 19. (original) The method of Claim 16 wherein the binary
2 operation is minimum finding operation.

1 20. (original) The method of Claim 16 wherein the binary
2 operation is a maximum finding operation.

1 21. (canceled)

1 22. (canceled)

1 23. (canceled)

1 24. (canceled)

1 25. (canceled)